Computer Science Comprehensive Exam

Architecture

January 13, 1997

This is a closed-book exam. You have 1.5 hours to complete it. Answer all of the questions. Be concise in your answers. You will receive partial credit for partially correct answers, but extraneous remarks may count against you.

1. Suppose you have an architecture similar to the MIPS, with 5 phases: Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory (MEM), and Write Back (WB). You are considering pipelining the execution of these stages to improve performance. Assume that you will have a 5-stage pipeline; one stage per phase. Also assume only an integer pipeline—don't worry about multiple EX stages for floating-point operations.

   (a) Give as many reasons as you can for why one cannot expect to obtain a speedup of 5 using this (5-stage) pipeline.

   (b) Explain what is meant by (1) structural hazards, (2) data hazards and (3) control hazards and the effect of such hazards upon pipeline speedup. Describe the hardware support required by the pipeline in order to minimize the effects of such hazards.

2. Suppose that you have been given the task of providing advice on the design of the cache memory for a new workstation. The machine is to have a single 64-bit processor.

   (a) Consider the following specific design issues. For each, define the issue, state what the choices are, and *briefly* discuss the tradeoffs between the alternative approaches.

   - one- vs. two-level cache
   - unified vs. separate i- and d-caches
   - cache organization and addressing method
   - cache write policy

   (b) Considering price, performance, and potential user applications, pick the combinations of choices you think would make sense for low-end and high-end models of the machine. Briefly justify your choices.

3. You are asked to evaluate two proposed ways of attaching a high-speed network adaptor to a computer system. In both cases, the adaptor physically plugs into the system's I/O bus.

   With approach A, the network adaptor contains 1 MByte of "outboard" memory that can be accessed (read/write) on a word-by-word basis across the I/O bus. The network adaptor can transmits outgoing messages from this memory, and can place incoming messages into predetermined regions of this memory at network speed.

   With approach B, the network adaptor contains no memory. Outgoing messages are transmitted from main memory via direct memory access (DMA). Incoming messages are placed into predetermined regions of main memory via DMA. Assume that the DMA can proceed at network speed.

(a) Briefly discuss all of the issues that influence your choice between these two approaches. What data would you need about the computer system and the expected usage of the network adaptor to make an informed decision?

(b) Assume that the network adaptor is intended to support a machine used as a departmental file server. Which approach of attaching the network adaptor is most appropriate in this case? Justify your answer.